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SCOTT C. HARRIS  
Fish & Richardson P.C.  
Suite 500  
4350 La Jolla Village Drive  
San Diego, CA 92122

EXAMINER

LEURIG, SHARLENE L

ART UNIT

PAPER NUMBER

2879

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/915,460

Applicant(s)

FUKUNAGA, TAKESHI

Examiner

Sharlene Leurig

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11 July 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5-8 and 19-21 is/are allowed.
- 6) ☒ Claim(s) 1-4, 9-18 and 22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 4.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Response to Amendment*

1. The Amendment filed on June 2, 2003 and the Supplemental Amendment filed on July 11, 2003 have been entered and acknowledged by the examiner. Claims 1-9 and 12-15 have been amended and claims 17-22 have been added.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 10, 14 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Yap (6,307,528).

Regarding claim 1, Yap discloses a light emitting device comprising a substrate (Figure 3a, element 42), a source wiring (Figure 4a, element 68) over the substrate, a gate wiring (66) over the substrate, at least one thin film transistor (Figure 4a, elements 46 and 70; Figure 3a, element 46) provided in an intersection of the source wiring and the gate wiring, an insulator (Figure 3a, element 52), a first electrode (54) formed on the insulator, a second electrode (62) formed on the insulator so as not to be in contact with the first electrode, and a light emitting layer (60) formed between the first and second

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electrodes on the insulator, wherein the thin film transistor is electrically connected to the first electrode by via (56).

Regarding claim 2, the first and second electrodes produce an electric field in a direction parallel with the insulator, which is a three-dimensional layer.

Regarding claim 3, Yap provides a switching thin film transistor (46) (column 8, line 26) and a current controlling thin film transistor (70) (column 8, line 35), which is electrically connected to the first electrode, in the intersection of the source and gate wirings.

Regarding claim 10, a film having some reflective properties (48) is provided under the light-emitting layer (60). The film (48) can be said to be reflective because it is described as a "low-reflectance film" (column 7, line 49), which is interpreted as meaning that it causes some reflection.

Regarding claim 14, Yap discloses a side surface of the first insulator layer (50) and a side surface of the second electrode (62) that are at an angle in relation to each other of between 30 and 90 degrees. Toward the center of the device in Figure 3a, the insulator layer (50) tapers off as the second electrode drops at an angle. Extending the two lines, the angle formed between the two is between 30 and 90 degrees.

Regarding claim 16, Yap discloses that the light-emitting device may be incorporated into a display device (column 1, lines 10-12).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-4, 9 and 16 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamada (6,246,179).

Regarding claim 1, Yamada discloses a light emitting device comprising a substrate (Figure 4b, element 10), a source wiring over the substrate, a gate wiring over the substrate (Figures 4, 4a and 4b, elements 51 and 52), at least one thin film transistor (33, 43) provided in an intersection of the source wiring and the gate wiring, an insulator (15, 32), a first electrode (61) formed on the insulator, a second electrode (67) formed on the insulator so as not to be in contact with the first electrode, and a light emitting layer (66) formed between the first and second electrodes on the insulator, wherein the thin film transistor is electrically connected to the first electrode (61).

Regarding claim 2, the first and second electrodes produce an electric field in a direction parallel with the insulator, which is a three-dimensional object.

Regarding claim 3, Yamada provides a switching thin film transistor (30) (column 5, line 6) and a current controlling thin film transistor (40) (column 5, line 11), which is electrically connected to the first electrode, in the intersection of the source and gate wirings.

Regarding claim 4, Yamada discloses a power supply line (Figure 4b, element 53) over the insulator (15, 32), a second insulator comprising resin (column 6, line 3) over the first insulator and the power supply line, a first electrode (61) formed on the

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second insulator, and a second electrode (67) formed on the second insulator so as not to be in contact with the first electrode.

Regarding claim 9, Yamada discloses the light emitting layer having an electron transport property and a hole transport property, as discussed above.

Regarding claim 16, Yamada discloses that the light-emitting device can be incorporated into a display device (column 1, line 7).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagayama et al. (5,742,129) in view of Yamada (6,246,179).

Regarding claim 1, Nagayama discloses a light emitting device comprising a substrate (Figure 3, element 2), a source wiring (column 5, line 57) over the substrate, a gate wiring (3) over the substrate, at least one thin film transistor (Figure 4, element 5) provided in an intersection of the source and gate wiring, an insulating layer as part of the thin film transistor array (column 5, line 55), a first electrode (Figure 3, element 6) formed over the thin film transistor array, a second electrode (9) provided on the insulator that is part of the thin film transistor array so as not to be in contact with the first electrode, and a light emitting layer (8) formed between the first and second electrodes

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on the insulator that is part of the thin film transistor array, wherein the thin film transistor is electrically connected to the first electrode.

Regarding claim 11, Nagayama discloses transparent layers as part of the thin film transistor array, which is formed on a transparent substrate, and a reflective layer (21) provided above the light-emitting layer.

Nagayama lacks disclosure of the insulating layer being formed over the thin film transistor or of the insulating layer being transparent.

Yamada teaches a light-emitting device having a thin film transistor with an insulating layer (Figure 4b, elements 12, 15) formed between the TFT and the first electrode in order to prevent electrical crosstalk between the elements of the transistor array and the electrode, while still providing controlled electrical contact between the TFT and the electrode. Yamada teaches yet another transparent insulating layer (17) which functions as a planarizing layer to smooth the surface of the thin film transistor array.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the light-emitting device of Nagayama to have an insulating layer in the thin film transistor array formed between the transistor and the electrode in order to smooth the surface of the transistor array and provide controlled electrical connection between the electrode and the TFT, and further for the insulator to be transparent in order to provide the desired effect, as taught by Yamada.

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8. Claims 12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagayama et al. (5,742,129) in view of Yamada (6,246,179) as applied to claims 1 and 11 above, and further in view of Haynes et al. (6,054,809) (of record).

Regarding claims 12 and 22, Nagayama discloses a light emitting device having an active TFT matrix including an insulating layer provided beneath a first electrode, but lacks disclosure of an insulator formed between the first electrode and the TFT.

Nagayama discloses a reflective layer (21) formed over the light-emitting layer (8).

Yamada teaches an insulator formed between a TFT and a first electrode and further teaches the insulator to be transparent.

Both Nagayama and Yamada lack disclosure of a reflective material for a reflective layer.

Haynes teaches a dielectric reflective layer formed of titanium oxide in a resin (column 9, lines 35-45) for a light-emitting device.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the light-emitting device of Nagayama to have an insulating layer in the thin film transistor array formed between the transistor and the electrode in order to smooth the surface of the transistor array and provide controlled electrical connection between the electrode and the TFT, and further for the insulator to be transparent in order to provide the desired effect, as taught by Yamada, and to further modify it to have the reflective layer formed of a resin containing titania, as taught by Haynes, to achieve the desired reflectance with a well-understood and readily available reflective material.



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9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yap (6,307,528).

Yap discloses a light-emitting device having all the limitations as discussed above in regard to claims 1-3. Yap discloses an insulating layer (Figure 3a, element 58) formed between the first electrode (54) and the second electrode (62) that is very thin in some areas, specifically where it tapers off toward the middle of the device.

Yap lacks explicit disclosure of the thickness of the single layer between the first and second electrodes.

It would have been obvious to one of ordinary skill in the art at the time of the invention to make an insulating layer of 200 nm or less in thickness, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the insulating layer disclosed by Yap to be 200 nm or less in thickness in order to make the device as thin and lightweight as possible, as it has been held to be within the ordinary skill of the art to modify thickness.

10. Claims 15, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (6,246,179) in view of Haynes et al. (6,054,809) (of record).

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Yamada discloses a light-emitting device having all the limitations discussed above in regard to claims 1-4, 9 and 16, including first and second electrodes.

Regarding claim 15, Yamada lacks disclosure of the first or second electrode being formed of gold, nickel, palladium, iridium or cobalt.

Haynes teaches that the first and second electrodes of a light-emitting device can be formed of a conductive material such as nickel (column 7, line 31).

Therefore regarding claim 15, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the light-emitting device of Yamada to have a first or second electrode formed of a conductive material such as nickel, as taught by Haynes, to achieve the desired conductance with a well-understood and readily available material.

Regarding claims 17 and 18, Yamada lacks disclosure of the first and second electrode being formed into either a comb tooth shape or a spiral shape on the insulator.

Haynes teaches a light-emitting device having a first and second electrode formed in a comb tooth shape where each tooth of the first electrode is adjacent to each tooth of the second electrode (Figure 11A) and a spiral shape (Figure 11B-D), where each tooth of the first electrode is engaged with those of the second electrode. Haynes teaches such a configuration in order to enable various lighting patterns, including complicated designs such as logos (column 16, lines 40-60).

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Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the light-emitting device disclosed by Yamada to have the desired brightness luminance patterns, as taught by Haynes.

11. Claims 15, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yap (6,307,528) in view of Haynes et al. (6,054,809) (of record).

Yamada discloses a light-emitting device having all the limitations discussed above in regard to claims 1-3, including first and second electrodes.

Regarding claim 15, Yap lacks disclosure of the first or second electrode being formed of gold, nickel, palladium, iridium or cobalt.

Haynes teaches that the first and second electrodes of a light-emitting device can be formed of a conductive material such as nickel (column 7, line 31).

Therefore regarding claim 15, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the light-emitting device of Yap to have a first or second electrode formed of a conductive material such as nickel, as taught by Haynes, to achieve the desired conductance with a well-understood and readily available material.

Regarding claims 17 and 18, Yap lacks disclosure of the first and second electrode being formed into either a comb tooth shape or a spiral shape on the insulator.

Haynes teaches a light-emitting device having a first and second electrode formed in a comb tooth shape where each tooth of the first electrode is adjacent to each

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tooth of the second electrode (Figure 11A) and a spiral shape (Figure 11B-D), where each tooth of the first electrode is engaged with those of the second electrode. Haynes teaches such a configuration in order to enable various lighting patterns, including complicated designs such as logos (column 16, lines 40-60).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the light-emitting device disclosed by Yap to have the desired brightness luminance patterns, as taught by Haynes.

#### ***Allowable Subject Matter***

12. Claims 5-8 and 19-21 are allowed.

13. The following is an examiner's statement of reasons for allowance: the prior art of record fails to disclose the combination of limitations as set forth in claims 5-8, and specifically the limitation of a light emitting device having a light emitting layer formed between an anode and a cathode, wherein the light emitting layer comprises a first layer having both an electron transport property and a hole transport property and a second layer containing a luminescent material, where the first layer is formed on the anode and the cathode and the second layer is formed on the first layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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***Response to Arguments***

14. Applicant's arguments with respect to claims 1-4, 9-18 and 22 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sharlene Leurig whose telephone number is (571) 272-2455. The examiner can normally be reached on Monday through Friday, 8:30am-5:00pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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**NIMESHKUMAR D. PATEL  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800**